**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. Cancelled

2. (Currently Amended) The processor of claim ~~1~~ 26, wherein each butterfly module includes a radix-2 butterfly unit and a feedback memory.

3. (Previously Presented) The processor of claim 2, wherein, for an input sequence of N samples, an output sequence $X(k,n)$ of each butterfly module is equal to $x(n)+(-1)^k x\left(n+\frac{N}{2}\right)$.

4. (Currently Amended) The processor of claim ~~1~~ 26, wherein at least one of the selectable multipliers for performing trivial coefficient multiplication is integrated in an adjacent butterfly module.

5. (Currently Amended) The processor of claim ~~1~~ 26, wherein the selectable multipliers each include a multiplier and a switch for bypassing the multiplier.

6. Cancelled

7. (Currently Amended) The processor of claim ~~6~~ 26, wherein the second and third butterfly modules are connected by ~~a selectable multiplier for performing trivial coefficient multiplication and~~ a selectable multiplier for performing the complex coefficient multiplication $W_N^{N/8}$.

8. (Previously Presented) The processor of claim 2, wherein, for an input sequence having $N$ samples, the feedback memories for the first, second and third butterfly modules hold $N/2$, $N/4$ and $N/8$ samples, respectively.

9. (Currently Amended) The processor of claim ~~1~~ 26 wherein the input sequence is of length $N$, where $(\log_2 N) \text{mod} 3 = 1$, the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having a butterfly unit and a corresponding memory sized to hold a single sample, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a butterfly operation on the received output sequence to render an FFT of the input sequence.

10. (Currently Amended) The processor of claim ~~1~~ 26 wherein the input sequence is of length $N$, where $(\log_2 N) \text{mod} 3 = 2$ , the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having first and second butterfly units having corresponding memories sized to hold two samples and a single sample respectively, the first butterfly unit connected to the second butterfly unit by a selectable multiplier for selectively multiplying the output of the first butterfly unit by $-j$, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a pair of butterfly operations on the received output sequence to render an FFT of the input sequence.

11. (Currently Amended) The processor of claim ~~1~~ 26, wherein the twiddle factor multiplier is a cordic rotator.

12. (Currently Amended) A pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of $N$ samples, the processor comprising:

at least one FFT triplet module, the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output sequence in accordance with a butterfly operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage module having a selectable multiplier for selectively multiplying the first stage output sequence by a trivial coefficient, wherein a selectable multiplier is selected in response to a first control signal provided by a first control circuitry with the second FFT stage module, the first control signal comprising a combination of a current and a prior switching signal, and a second stage radix-2 butterfly unit ~~for~~ controlled by the switching signal and providing a second stage output sequence in accordance with the butterfly operation performed

on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto; and

a third FFT stage module having a multiply selectable multiplier for selectively multiplying the second stage output sequence by at least one of the trivial coefficient and a complex coefficient, wherein a selectable multiplier is selected in response to a second control signal provided by a second control circuitry with the third FFT stage module, the second control signal comprising a combination of a current and a prior switching signal, a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the multiply selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence.

13. (Original) The FFT processor of claim 12, wherein each of the first, second and third stage output sequences $X(k,n)$ is equal to $x(n)+(-1)^k x\left(n+\frac{N}{2}\right)$.

14. (Previously Presented) The FFT processor of claim 12, wherein at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input sequence.

15. (Currently Amended) A pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of $N$ samples, the processor comprising:

at least one FFT triplet module, the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output sequence in accordance with a butterfly operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage module having a multiply selectable multiplier for selectively multiplying the first stage output sequence by at least one of the trivial coefficient and a constant complex coefficient, , ~~the selection being responsive~~ wherein a selectable multiplier is selected in response to a ~~step counter~~ first control signal provided with the second FFT stage module, the

first control signal comprising a combination of a current and a prior switching signal, ~~provided with the second FFT stage module,~~ and a second stage radix-2 butterfly unit responsive to the current switching signal for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto; and

a third FFT stage module having a selectable multiplier for selectively multiplying the second stage output sequence by a trivial coefficient, ~~the selection being responsive~~ wherein a selectable multiplier is selected in response to a ~~step counter~~ second control signal provided with the third FFT stage module, the second control signal comprising a combination of a current and a prior switching signal, ~~provided with the third FFT stage module,~~ a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence.

16. (Original) The FFT processor of claim 15, wherein each of the first, second and third stage output sequences $X(k,n)$ is equal to $x(n)+(-1)^k x\left(n+\frac{N}{2}\right)$.

17. (Previously Presented) The FFT processor of claim 15, wherein at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input sequence.

18. (Original) The FFT processor of claim 15, further including an FFT terminator determined in accordance with the length $N$ of the input sequence.

19. (Original) The FFT processor of claim 18, wherein the FFT terminator includes a butterfly module having a memory sized to store a single sample, for receiving as a terminator input, the output of the third FFT stage multiplier and for performing a butterfly operation on the terminator input to render an FFT of the input sequence of $N$ samples.

20. (Original) The FFT processor of claim 18, wherein the FFT terminator includes a first butterfly module having a memory sized to store a pair of samples, for receiving as a

terminator input, the output of the third stage multiplier and for performing a butterfly operation on the terminator input, and a second butterfly module connected to the first butterfly module of the terminator by a selectable multiplier, the selectable multiplier for selectively multiplying the output of the first butterfly module of the terminator by *-j*, the second butterfly module having a memory sized to store a single sample and for performing a butterfly operation on the selectively multiplied output of the first butterfly module of the terminator to render an FFT of the output sequence.

21. (Currently Amended) A method of performing an FFT on a data sequence of $N$ samples in an FFT processor having a butterfly module, the method comprising:

for all integers x according to $1 \leq x \leq \log_2 N$, repeating the steps of

receiving and buffering $\frac{N}{2^x}$ samples at a time from a sequence having $N$ samples;

generating a 2-point FFT using the $n^{th}$ and the $\left(2+\frac{N}{2^x}\right)^{th}$ samples;

~~responsive to a step-counter provided with the butterfly module,~~ selectively multiplying the generated 2-point FFT sequence by a complex valued multiplicand, wherein a multiplier for selectively multiplying is selected in response to a control signal provided with each butterfly module, the control signal comprising a combination of a current and a prior switching signal;

terminating the FFT using a termination sequence determined in accordance with a ($\log_2 N$)mod3 relationship[~~,~~] to obtain an FFT of the sequence of N samples; and

outputting the FFT of the sequence of N samples.

22. (Previously Presented) The method of claim 21 wherein the complex valued multiplicand is selected from a list including 1, *-j*, $\frac{\sqrt{2}}{2} - j\frac{\sqrt{2}}{2}$, and a complex twiddle factor coefficient.

23. (Original) The method of claim 21 wherein ($\log_2 N$)mod3 =1 and the step of terminating the FFT includes buffering a sample received from the final selective multiplication and performing a 2-point FFT using the buffered sample and the subsequent sample in the sequence to obtain the FFT of the sequence of $N$ samples.

24. (Original) The method of claim 21 wherein $(\log_2 N) \text{mod} 3 = 2$ and the step of terminating the FFT includes:

buffering a pair of samples received from the final selective multiplication and performing pair-wise 2-point FFTs using the two buffered samples and the two subsequent samples in the sequence;

selectively multiplying the result of the pair-wise 2 point FFT by *-j*; and

buffering a sample received from the selective multiplication of the pair-wise 2-point FFT and performing a 2-point FFT using the buffered sample and the subsequent sample in the sequence to obtain the FFT of the sequence of N samples.

25. (Previously Presented) The FFT processor of claim 12, further including an FFT terminator determined in accordance with the length N of the input sequence.

26. (New) A pipelined fast Fourier transform (FFT) processor for receiving an input sequence, the processor comprising:

a first butterfly module for receiving a first input data sequence and outputting a first output data sequence;

a first selectable multiplier coupled to receive the first output data sequence from the first butterfly module and configured to selectively perform trivial coefficient multiplication and complex coefficient multiplication on the first output data sequence to generate a second input data sequence in response to a first control signal;

a second butterfly module coupled to receive the second input data sequence from the first selectable multiplier and output a second output data sequence in response to a second switching signal, the second butterfly module having a first control circuitry configured to generate the first control signal in response to the current state of the second switching signal and the prior state of the second switching signal;

a second selectable multiplier coupled to receive the second output data sequence from the second butterfly module and configured to selectively perform trivial coefficient multiplication and complex coefficient multiplication on the second output data sequence to generate a third input data sequence in response to a second control signal;

a third butterfly module coupled to receive the third input data sequence from the second selectable multiplier and output a third output data sequence in response to a third switching signal, the third butterfly module having a second control circuitry configured to generate the second control signal in response to the current state of the third switching signal and the prior state of the third switching signal;

a twiddle factor multiplier coupled to receive the third output data sequence from the third butterfly module, apply a twiddle factor to the third output data sequence and provide a final output data sequence which represents an FFT of the first input data sequence; and

wherein the first and second control circuitry reduce the complexity and size of the FFT processor.